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L10	5	9 and switch\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/20 17:52
L11	39	9 not 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/20 18:00
L12	107	708/620,402,624,700.ccls. and Booth	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/20 18:01
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Kunimatsu, A.; Ide, N.; Sato, T.; Endo, Y.; Murakami, H.; Kamei, T.; Hirano, M.; Ishihara, F.; Tago, H.; Oka, M.; Ohba, A.; Yutaka, T.; Okada, T.; Suzuoki, M.;

Micro, IEEE ,Volume: 20 , Issue: 2 , March-April 2000

Pages:40 - 47

[Abstract] [PDF Full-Text (136KB)] **IEEE JNL**

2 A microprocessor with a 128-bit CPU, ten floating-point MAC's, four floating-point dividers, and an MPEG-2 decoder

Suzuoki, M.; Kutaragi, K.; Hiroi, T.; Magoshi, H.; Okamoto, S.; Oka, M.; Ohba, A.; Yamamoto, Y.; Furuhashi, M.; Tanaka, M.; Yutaka, T.; Okada, T.; Nagamatsu, M.; Urakawa, Y.; Funyu, M.; Kunimatsu, A.; Goto, H.; Hashimoto, K.; Ide, N.; Murakami, H.; Ohtaguro, Y.; Aono, A.;

Solid-State Circuits, IEEE Journal of ,Volume: 34 , Issue: 11 , Nov. 1999

Pages:1608 - 1618

[Abstract] [PDF Full-Text (640KB)] **IEEE JNL**

3 A microprocessor with a 128 b CPU, 10 floating-point MACs, 4 floating-point dividers, and an MPEG2 decoder

Kutaragi, K.; Suzuoki, M.; Hiroi, T.; Magoshi, H.; Okamoto, S.; Oka, M.; Ohba, A.; Yamamoto, Y.; Furuhashi, M.; Tanaka, M.; Yutaka, T.; Okada, T.; Nagamatsu, M.; Urakawa, Y.; Funyu, M.; Kunimatsu, A.; Goto, H.; Hashimoto, K.; Ide, N.; Murakami, H.; Ohtaguro, Y.; Aono, A.;

Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC.

1999 IEEE International , 15-17 Feb. 1999

Pages:256 - 257

[Abstract] [PDF Full-Text (164KB)] **IEEE CNF**

4 A high bandwidth superscalar microprocessor for multimedia applications

Raam, F.M.; Agarwal, R.; Malik, K.; Landman, H.A.; Tago, H.; Teruyama, T.; Sakamoto, T.; Yoshida, T.; Yoshioka, S.; Fujimoto, Y.; Kobayashi, T.; Hiroi, T.; Oka, M.; Ohba, A.; Suzuoki, M.; Yutaka, T.; Yamamoto, Y.;

Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC.

1999 IEEE International , 15-17 Feb. 1999

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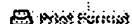
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1 A painless way to reduce power dissipation by over 18% in Booth-encoded carry-save array multipliers for DSP

Zhan Yu; Wasserman, L.; Willson, A.N., Jr.;

Signal Processing Systems, 2000. SIPS 2000. 2000 IEEE Workshop on , 11-13 Oct. 2000

Pages:571 - 580

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Goto, G.; Inoue, A.; Ohe, R.; Kashiwakura, S.; Mitarai, S.; Tsuru, T.; Izawa, T.;

Solid-State Circuits, IEEE Journal of , Volume: 32 , Issue: 11 , Nov. 1997
 Pages:1676 - 1682

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2 Circuit techniques for CMOS low-power high-performance multipliers

Abu-Khater, I.S.; Bellaouar, A.; Elmasry, M.I.;

Solid-State Circuits, IEEE Journal of , Volume: 31 , Issue: 10 , Oct. 1996
 Pages:1535 - 1546

[\[Abstract\]](#) [\[PDF Full-Text \(936 KB\)\]](#) **IEEE JNL**
3 A 4.1 ns compact 54x54 b multiplier utilizing sign select Booth encoders

Inoue, A.; Ohe, R.; Kashiwakura, S.; Mitarai, S.; Tsuru, T.; Izawa, T.; Goto, G.;

Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC., 1997 IEEE International , 6-8 Feb. 1997
 Pages:416 - 417, 497

[\[Abstract\]](#) [\[PDF Full-Text \(424 KB\)\]](#) **IEEE CNF**
4 A new approach for high performance multiply-accumulator design

Lan Jinghong; Ji Lijiu; Jiang Anping; Jia Song;

ASIC, 2003. Proceedings. 5th International Conference on , Volume: 2 , 21-24 Oct. 2003
 Pages:1293 - 1295 Vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(244 KB\)\]](#) **IEEE CNF**
5 Design of a high performance 32x32-bit multiplier with a novel sign select Booth encoder

Kiwon Choi; Minkyu Song;

Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on , Volume: 2 , 6-9 May 2001
 Pages:701 - 704 vol. 2

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